IPC3: H 04 Q 3/52
FEDERAL REPUBLIC OF GERMANY H 03 K 17/16

H 03 K 17/693

GERMAN
PATENT OFFICE

OFFENLEGUNGSSCHRIFT DE 31 51 080 A1

Reference: P 31 51 080,9
Application date: 12/23/81
Laid open to public inspection: 7/14/83

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Request for examination is made under § 44 of the Patent Law

Title: Cross-Point Device

The crosstalk damping in the case of high frequencies should be improved in a cross-point device with field effect transistors as coupling elements. To this end a second MOS field effect transistor is connected in each cross-point array in such a manner that the source-gate stray capacitances remain active in the blocked state of the coupling element as reactances and form a capacitive voltage divider with a drain-source partial capacitor. (31 51 080)

CLAIMS:

1. A cross-point device with field effect transistors as coupling elements, in which the gate connections and the bulk connections of the field effect transistors are on AC reference potential and the drain-source stretches are the patchable signal stretches, characterized in that each coupling element (5 to 8) comprises, in addition to a first field effect transistor (F1), a second field effect transistor (F2), that both field effect transistors are MOS field effect transistors (F1, F2), that the drain-source stretch of the second field effect transistor (F2), whose gate-and bulk connections are on reference potential (1), is connected in series to the drain-source stretch of the first field effect transistor (F) so that the drain-and/or source-gate partial capacitors (C_D, C_S) are parallel, and that these partial capacitors are maintained active in the blocked state of the coupling element (5 to 8) between the source- and drain connection point of the two field effect transistors (F1, F2) and between the reference potential (1) as reactance and form a capacitive voltage divider with a drain-source partial capacitor (C1) of the second field effect transistor (F2).

2. The cross-point device according to Claim 1, characterized in that the two field effect transistors (F1, F2) are connected to one another at their source connections (S).

3. The cross-point device according to Claim 1 or 2, characterized in that a capacitor (C2) is connected in between the common connection point of the two field effect transistors and the reference potential (1).

4. The cross-point device according to Claim 3, characterized in that a resistor (R1) is connected in series with the capacitor (C1).

Cross-Point Device

The invention is relative to a cross-point [switching] device in accordance with the generic part of Claim 1.

Such a cross-point device is described in DE 19 22 382. In it the patchable transmission stretch is formed by the drain-source stretch of a single field effect transistor. The partial capacitors between the electrodes that are obligatorily present in the latter are rendered inactive by an additional capacitance so that a good decoupling is achieved between the input and the output of the coupling element even at high frequencies. In order to keep the capacitive crosstalk between patch connections as low as possible, amplifiers are provided in the input lines that have the lowest possible internal resistance on their output

Crosstalk is a function of the partial capacitor of the drain-source stretch that determines the resistance of the cut-out coupling element, even though this partial capacitor is very small. It can be lowered to a value of approximately 0.03 pF by special screening measures. Nevertheless, a crosstalk attenuation results at high frequencies, e.g., 20 MHz, that is so low that the coupling element cannot be used in broad-band carrier frequency systems.

DE-OS 26 54 269 teaches a circuit arrangement with three field effect transistors in which the drain-source stretches of two transistors are connected in series and the third transistor switches to ground as a transverse

[cross, shunt] transistor. Such a circuit arrangement is expensive on account of the third field effect transistor and cannot be realized at the present on account of the spatial expansion for high frequencies and sufficient crosstalk attenuation.

A similar circuit is shown in figure 2 of DE-AS 12 380 891. In figure 1 of this published, examined application a low-resistive resistor connects the source- and the gate connections of two field effect transistors. The influence of the partial capacitors should be reduced therewith in the patched state in order to achieve a higher switching speed as well as a higher transmission frequency. However, this causes a significant damping of the signal in the patched coupling element.

The invention has the problem of designing a circuit in accordance with the generic part of Claim 1 in such a manner that the crosstalk damping is distinctly improved at high frequencies.

The above problem is solved by the features of the characterizing part of Claim 1.

It is surprising in the circuit in accordance with the invention that a substantial improvement of the crosstalk damping results in the high-frequency range with only two MOS field effect transistors. This is achieved by making use of partial capacitors between the electrodes, that are suppressed in the state of the art.

Embodiments of the invention result from the following description.

Figure 1 shows a cross-point [switching] array.

Figure 2 shows a coupling element of the cross-point array.

Figure 3 shows an equivalent circuit diagram of the patched coupling element according to figure 2.

Figure 4 shows an equivalent circuit diagram of the series connection of a blocked [suspended] coupling element and of a patched coupling element in accordance with figure 2.

Figure 5 shows an equivalent circuit diagram for the instance of only one field effect transistor as coupling element.

Figure 6 shows another exemplary embodiment of a coupling element.

In the asymmetric cross-point array according to figure 1 four ground-symmetric coupling elements 5 to 8 are provided for connecting the four rails [bars, tracks] 1 to 4. A voltage source Q1 is on an input E1 of rail 1. A voltage source Q2 is on input E2 of rail 2. Both voltage sources Q1, Q2 have an internal resistance Ri of approximately 0Ω. Amplifier V1 is on output A1 of rail 3. Amplifier V2 is on output A2 of rail 4. Input resistance Re of amplifiers V1 and V2 is substantially greater than the patch [through] resistance Rd of coupling elements 5 to 8.

Each coupling element 5 to 8 has two MOS field effect transistors F1 and F2 (figure 2). Drain connection D of field effect transistor F1 is on rail 1 for coupling elements 5, 6 and on rail 2 for coupling elements 7, 8. Drain connection D of field effect transistor F2 is connected to rail 4 for coupling

elements 5, 7 and to rail 3 for coupling elements 6, 8. Source connections S of field effect transistors F1, F2 are connected to one another so that the drain-source stretches of the two field effect transistors F1, F2 are in series between the rails. Gate connections G of field effect transistors F1, F2 are connected to the reference potential with control input St and via a capacitor (that is, with alternating current). Bulk connections B of field effect transistors F1, F2 are on their gate connections G. The circuit that cuts coupling elements 5 to 8 in and out on input St is not shown in detail.

It is assumed in order to describe the method of operation of the circuit according to figure 2 that coupling elements 6, 7 are patched and coupling elements 5, 8 are blocked. Input E1 is connected to output A1 and input E2 to output A2 therewith. This wires a path I and a path II.

In this instance crosstalk occurs in particular via coupling element 8 from path II to path II. This crosstalk path II/I is indicated in dotted lines in figure 1.

Figure 4 shows the equivalent circuit diagram of crosstalk path II/I with the partial capacitors of field effect transistors F1, F2 active at the higher signal frequencies. Partial capacitors C_D are active on drain connections D and partial capacitors C_S are active on the source connections. Partial capacitors C_I occur between the drain connections and the source connections. These partial capacitors are shown in figure 4 solely in the case of field effect transistors F1, F2 of blocked coupling element 8, that forms the complex blocking [reverse] resistance by the partial capacitors and

the high-resistive blocking resistances $R_{aus\ [=out]}$. The corresponding partial capacitors are not shown in patched coupling element 6 in figure 4 since they have practically no effect. Only the low-resistive connecting resistors $R_{ein\ [in]}$ ($Rd = 2R_{ein}$) of the two field effect transistors F1 and F2 are shown. Figure 3 shows the partial capacitors of a patched coupling element.

The following applies for crosstalk damping a_N on the voltage divider, as it is shown in figure 5 with complex resistors $Z_{aus\ [out]}$ and $Z_{ein\ [in]}$:

$$a_N = 20\ lg \left| U_1 / U_2 \right| \approx 20\ lg \left| Z_{aus} / Z_{ein} \right| \text{ in dB.}$$

As can be seen from figure 4 two voltage dividers result in the equivalent circuit, namely, between voltages U_1 and U_2' on the one hand and voltages U_2' and U_2 on the other hand. Accordingly, the logarithmic damping values of these two voltages dividers are summed together so that the following results for crosstalk damping a_{N4} in the case of figure 4:

$$a_{N4} = 20\ lg \left| U_1 / U_2' \right| + 20\ lg \left| U_2' / U_2 \right|$$

$$\approx 20\ lg \left| \frac{2\ CS}{C1} \right| + 20\ lg \left| \frac{1}{2R_{ein}\ \omega\ C_1} \right| \text{ in dB,}$$

in which the last-cited relationship is a formulation for high frequencies, e.g., 20 MHz, in which switching element operations to be disregarded are eliminated.

A type B5V 81 MOS field effect transistor has the following values according to data sheet at 1 MHz:

$C_{SG} \leq 0.5$ pF $\qquad R_{ein\ [in]} = 40\Omega$

$C_{DG} \leq 1.2$ pF $\qquad R_{aus\ [out} = 100\ M\Omega_]$

$C_{GB} \leq 5$ pF

In a practically constructed circuit the following results using MOS field effect transistors of the cited type at 20 MHz capacitance values:

$C_1 \approx 0.03$ pF,
$C_S \approx 3$ pF, which, conditioned by the circuit design, is greater than capacitance C_{SG}.

A crosstalk damping a_{N4} of approximately 112 dB results from these capacitance values taking into consideration the above formula at 20 MHz.

If this value is compared with the crosstalk damping that would occur if the coupling element had only one MOS field effect transistor, the result is that one would then have to reckon only with a crosstalk damping a_{N1} of approximately 76 dB. This is due to the fact that in the last-cited instance the partial capacitance C_S remains practically without influence on the crosstalk damping. Crosstalk damping a_{N1} would result in this instance, in which the coupling element has only one field effect transistor, from:

$$A_{N1} \approx 20 \lg \frac{1}{R_{ein[in]}\,\omega\, C_1} \text{ in dB,}$$

In which the first summation part of a_{N4}, into which partial capacitances C_1 and $2C_6$ enter, obviously does not occur.

This creates a cross-point array with only two MOS field effect transistors per coupling element which array is suitable for patching broad-band signals with high crosstalk damping. Even at frequencies of 36 MHz and higher the circuit of the invention still achieves a substantial improvement of crosstalk damping compared to only one field effect transistor per coupling element.

The following table collates the results:

	1 FET	**2 FET**	**improvement**
A_N at 20 MHz	**76 dB**	112 dB	**36 dB**
A_N at 36 MHz	**73 dB**	**109 dB**	**36 dB**

It can be advantageous in a further development of the invention in order to improve the blocking behavior at lower frequencies to provide an additional capacitor C2 or a capacitor-resistor combination C2, R1 parallel to the parallel circuit of partial capacitors C_S. However, this results in an influencing of the frequency response of the patched coupling element (see figure 3) that must be considered. Figure 6 shows such a circuit.

Source connections S are connected together in the above exemplary embodiment. In another embodiment of the invention the drain connections can be on each other instead, in which case the capacitors decisive for improving the crosstalk damping are the capacitors C_D.

It is also possible to connect drain connection D of the one field effect transistor to the source connection of the other field effect transistor. Then, capacitor C_D of the one field effect transistor and capacitor C_S of the other one are active for the improving of the crosstalk damping. The polarity of field effect transistors F1, F2 can also be selected in accordance with the requirements of the particular application. However, care is to be taken that the selected circuit of partial capacitors C_S and C_D effects the frequency response in the cut-in state.

Patent Translations

German, French, Dutch, Swedish

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April 25, 2004

INVOICE #3011

Attn.: Heather L. Adamson, Paralegal

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Adamson, Heather L.

From: Klindtworth, Jason K.
Sent: Tuesday, April 27, 2004 2:32 PM
To: Adamson, Heather L.
Cc: Houk, Sally
Subject: RE: New Real File

Date: 4/26/2004
Client: 109905 REALNETWORKS INC
Matter: 109905-137512 RN105 SYSTEM AND METHOD OF ORGANIZING AND
Billing Tmkpr: Klindtworth, Jason K

-----Original Message-----
From: Adamson, Heather L.
Sent: Tuesday, April 27, 2004 2:04 PM
To: Houk, Sally
Cc: Klindtworth, Jason K.
Subject: RE: New Real File

Sally, have we rec'd a c/m# yet?

thanks!

-----Original Message-----
From: Klindtworth, Jason K.
Sent: Wednesday, April 21, 2004 3:10 PM
To: Adamson, Heather L.; Houk, Sally
Subject: New Real File

Sally,
Can you please open a new RealNetworks file entitled "RN105 SYSTEM AND METHOD OF ORGANIZING AND EDITING METADATA"
PBA=JKL;SUP=JKL;COL=JKL,ATA

and print out the attached documents when you have a second.

Heather,
Please docket a 2 month date and a 3 month date.

<< Message: RE: REALNET.105A >> << Message: Fwd: REALNET.105A >>

Thanks!

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